CLAIMS:

What is claimed:

1. An integrated circuit comprising:

a first port for outputting a signal;

a second port for receiving said signal;

an alignment link for electrically connecting said first port with said second port; and

said alignment link comprises a signal buffer for buffering a signal traveling along said alignment link between said first port and said second port.

2. An integrated circuit according to claim 1 wherein said alignment link further comprise a wiring trace.

3. An integrated circuit according to claim 1 wherein said alignment link comprises a common area of integrated circuit real estate.

4. An integrated circuit according to claim 1 wherein said first port is located in a first area of integrated circuit real estate.

5. An integrated circuit according to claim 1 wherein said second port is located in a second area of integrated circuit real estate.

6. An integrated circuit according to claim 1 wherein said integrated circuit real estate comprises multi-levels.

7. An integrated circuit according to claim 6 wherein said multi-levels comprise a semiconductor level and a wire tracing level.

8. An integrated circuit according to claim 7 wherein said semiconductor level comprises said signal buffer.

9. An integrated circuit according to claim 7 wherein said wire-tracing level comprises said first port and said second port.

10. An integrated circuit according to claim 9 wherein said wire-tracing level comprises a plurality of levels.

11. A method of aligning ports in an integrated circuit comprising the steps of:

extending a first port from one area into a common area;

extending a second port from a second area into said common area; and

linking said first port to said second port within said common area via an alignment link wherein said alignment link comprises a wiring trace and a signal buffer.

12. A method of aligning ports in an integrated circuit according to claim 11 wherein said common area comprises a multi level area.

13. A method of aligning ports in an integrated circuit according to claim 12 wherein said multi-level area comprises a wiring level and a semiconductor level.

14. A method of aligning ports in an integrated circuit according to claim 13 wherein said semiconductor level comprises said signal buffer.

15. A method of aligning ports in an integrated circuit according to claim 13 wherein said wiring level comprises said wiring trace.

16. A method of aligning ports in an integrated circuit according to claim 11 wherein said first area and said second area are at a substantial distance from each other relative to overall integrated circuit real estate.

17. An integrated circuit comprising :

a first port for outputting a signal;

a second port for receiving said signal; and

an alignment means for electrically connecting said first port with said second port.

18. An integrated circuit according to claim 17 wherein said alignment means comprises a wiring trace and signal buffering circuitry.

19. An integrated circuit according to claim 18 wherein said wiring trace and said signal buffering circuitry occupy a common area of integrated circuit real estate.

20. An integrated circuit according to claim 19 wherein said first port and said second port are located at a substantial distance to each other relative to overall integrated circuit real estate.